On page 47, line 2, delete "Figure 8" and substitute --Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute --from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Sub B'

151. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

issuing a read request to the memory device, wherein in response to the read request, the memory device outputs first and second portions of data onto a bus;

sampling the first portion of data from the bus synchronously with respect to a rising edge transition of an external clock signal; an

sampling the second portion of data from the bus synchronously with respect to a falling edge transition of the external clock signal.

152. The method of claim 151 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device onto a bus in response to the read request; wherein

a first portion of the amount of data is sampled from the bus synchronously with respect to a rising edge transition of an external clock signal; and

a second portion of the amount of data is sampled from the bus synchronously with respect to a falling edge transition of the external clock signal.

153. The method of claim 152 wherein, in response to the read request, the first portion of the amount of data is output onto the bus after a delay time transpires.

154. The method of claim 153 further including providing access time information to the memory device.

155. The method of claim 154 wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the first portion of the amount of data is output onto the bus.

156. The method of claim 151 wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

157. A controller device for controlling a synchronous memory device, the controller device comprising:

output driver circuitry to output a read request to the memory device, wherein in response to the read request, the memory device outputs a first and second portion of data onto a bus; and

input receiver circuitry to sample the first portion of data from the bus synchronously with respect to a rising edge transition of the external clock signal and a second portion of data from the bus synchronously with respect to a falling edge transition of the external clock signal.

158. The controller device of claim 157 wherein the input receiver circuitry includes first latch circuitry to latch the first portion of data, and second latch circuitry to latch the second portion of dat

159. The controller device of claim 157 further including a delay lock loop circuit coupled to the external clock signal, the delay lock loop circuit generating a first internal clock signal, wherein the input receiver circuitry samples the first portion of data in response to the first internal clock signal.

160. The controller device of claim 159 wherein the delay lock loop circuit generates a second internal clock signal, wherein the

input receiver circuitry samples the second portion of data in response to the second internal clock signal.

161. The controller device of claim 157 wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

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162. The controller device of claim 157 wherein the input receiver circuitry samples an amount of data during a plurality of clock cycles of the external clock signal.

163. The controller device of claim 162 wherein the output driver circuitry provides information representative of the amount of data to output in response to a read request to the memory device.

164. The controller device of claim 163 wherein the read request and the information representative of the amount of data to output are included in a read request packet.

165. A method of operation of a memory controller device comprising:

issuing a write request to a memory device synchronously with respect to an external clock signal, wherein in response to the write request, the memory device inputs first and second portions of data

outputting the first portion of data synchronously with respect to a first edge transition of an external clock signal; and

outputting the second portion of data from the bus synchronously with respect to a second edge transition of the external clock signal.

166. The method of claim 165 wherein the controller device outputs the first portion of data after a delay time transpires.

sub B'

167. The method of claim 165 further including providing access time information to the memory device.

168. The method of claim 167 wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the first portion of the amount of data is available on a bus.

169. The method of claim 165 wherein the first and second edge transitions of the external clock signal include voltage swings of less than one volt.

170. The method of claim 165 wherein the first portion of data and second portion of data include voltage swings of less than one volt

171. The method of claim 165 wherein the data is output during a plurality of first and second edge transitions of the external clock signal.

172. The method of claim 165 further including providing block size information to the memory device, wherein the block size